Thermal and electronic analysis of GaInAs/AlInAs mid-IR QCLs

Gaetano Scamarcio
Miriam S. Vitiello, Vincenzo Spagnolo, Antonia Lops

Regional Laboratory LIT³, CNR - INFM
Physics Dept., University of Bari, Italy

T. Gresch, J. Faist
University of Neuchatel → TU Zurich

Acknowledgements:
Q. Yang, J. Wagner
Fraunhofer Inst. Freiburg
Motivation

• > 10 years progress in the quantum design of active regions → high performance QCLs (CW, RT, single mode, high power, at selected mid-IR λ’s)

• Real-world applications want improved performance:
  – e.g. ppb/ppt QCL-based sensor systems compact/portable, affordable, battery-operated, ...

• “Typical” QCLs have:
  – Large electrical power (~ 10 W)
  – Low wall-plug efficiencies at room temperature (single-digit %)

• Heat generated in the active not efficiently extracted from the device
  – Physical limits → (thermal boundary resistance) (# interfaces)
RT CW mid-IR QCLs fabrication technologies

**Electroplated QCLs**
- Heat extraction in all in-plane directions
- Au top contact layer width > 4 µm

**InP-buried QCLs**
- Lateral heat extraction enhanced
- Require additional growing steps
- May suffer from current leakage

**Epilayer-down QCLs**
- Better coupling w/ heat sink
- High quality wafer bonding required

**State-of-art** [Evans, Slivken, Razeghi et al. APL, Aug.2007]

Narrow-ridge buried heterostructure waveguides + Electroplating + Thermally optimized packaging

*9.3% wall-plug efficiency at RT at 4.7 µm (!)*
Outline

• Review on thermal properties of mid-IR QCLs
  – focus on devices operating in the 3-5 µm window
  – GaInAs/AlInAs
  – GaInAs/AlGaAsSb

• Strategies to improve thermal performance of mid-IR QCLs
  – InAs/InGaAs AlAs/AlInAs smoothed interfaces
  – Improved processing using high-k dielectrics

• Assessment of the electronic and thermal properties of mid-IR QCLs via µ-probe photoluminescence
  – Electron lattice coupling vs conduction band offset
  – Thermal boundary resistance
Experimental approach

• Photoluminescence spectroscopy on the laser *front facets*

• Exploit
  – *µ-probe* spatial resolution (diffraction limit)
  – No hot-spots or surface e-h recombination (unipolarity)

• Facet temperatures close to bulk temperature in QCLs

• Photoluminescence analysis
  – Local *lattice and electronic temperatures*
Anisotropic thermal conductivity
2D thermal modeling

[Lops, Spagnolo, Scamarcio, JAP 2006]

GaInAs/AlInAs mid-ir QCLs @ 8.1 µm

- $T_L > T_H$: Temperature overshoot in the active region $\Rightarrow k_\perp$
- $\Delta T$ across the active $\Rightarrow$ different heat fluxes towards AlInAs cladding and InP substrate
- Modeling $\Rightarrow k_\perp = 0.6 \text{ W/K m}$ one order of magnitude smaller than bulk (!?!?!)
Thermal conductivity extraction

\(- \nabla \cdot (k \nabla T) = Q\)

- 2D-heat transport eq. solved and fitted to the exp data
- Boundary conds.: \(T = T_H\); no heat escapes through the sides or top of the laser
- Known conductivities for all bulk-like layers considered
- Temperature influence and doping influence included
- Only fitting parameters: \(k_\perp\) and \(k_\parallel\) in the active region
Thermal resistivity in heterostructures

- If $N$ small $\rightarrow$ interface contribution to $R$ is negligible

- Our experiments in THz and mid-IR QCLs:
  - *bulk contribution never accounts for the measured values*
  - Interface thermal resistivity dominant

- Comparing experimental $R$ with calculated bulk contributions $\rightarrow$ TBR

\[
R = \frac{a}{a+b} R_a + \frac{b}{a+b} R_b + \frac{N}{a+b} TBR
\]

$a, b$: well, barrier thickness

# interfaces

Thermal boundary or Kapitza resistance

Weighted average of bulk resistivities

Interface thermal resistivity
Can we improve the thermal conductivity of mid-IR QCLs?

- Design active regions with reduced TBR
  - material choice
  - reduce interface sharpness

- Improve device fabrication
  - use of high-$k$ dielectrics
Influence of material: the case of InGaAs/AlGaAsSb active regions

[calculations by C. Zhu et al. JAP (2006)]

- $K(\text{AlGaAsSb}) \approx \frac{1}{4} K(\text{InGaAs}), K(\text{InAlAs})$
  however
- Better matching of phonon properties in InGaAs/AlGaAsSb
  - phonon dispersion; acoustic impedance (mass density x sound velocity); phonon DOS; Debye temperature
- $\rightarrow TBR (\text{InGaAs}/\text{AlGaAsSb}) < TBR (\text{InGaAs}/\text{AlInAs})$
InGaAs/AlGaAsSb QCLs
[Vitiello, Scamarcio, Spagnolo, Yang, Wagner et al. APL, 2007]

- Emission wavelength $\lambda = 4.9 \mu m$
- # interfaces = 550
- $k_\perp = 1.8 \text{ W/K}\cdot\text{m}$
- Interface contribution to thermal resistivity = 63%
- $TBR = 0.75 \times 10^{-9} \text{ K/W}\cdot\text{m}^2$
  - Comparable with GaAs/AlGaAs
  - ~ 5 times better than GaInAs/AlInAs
Influence of interface structure

[Vitiello, Gresch, Spagnolo, Scamarcio, Faist et al., submitted APL, 2007]

- Strained $\text{In}_{0.61}\text{Ga}_{0.39}\text{As}/\text{In}_{0.45}\text{Al}_{0.55}\text{As}$ QCLs
- InAs or AlAs $\delta$-layers (0.2 nm) to increase the conduction band discontinuity in the active layers
- 1ML broadening at IFs included in the design
- Emission wavelength $\lambda = 4.78 \mu m$
- Peak optical power: 0.55 W @ 323 K; $T_{\text{MAX(CW)}} = 243$ K
• $k_L = 2.0 \text{ W/K}\cdot\text{m}$
• # interfaces = 600 / 1325
• $TBR = 0.5 - 1.1 \times 10^{-9} \text{ K/W}\cdot\text{m}^2$
  – Comparable with GaAs/AlGaAs

Temperature mapping

$T_L (K)$ vs. $z (\mu\text{m})$ for $P=4\text{W}$

- Centre
- Side

InGaAs
InGaAs
InGaAs
InP
AR
SiO$_2$

InP

5µm Au
Mid-ir InGaAs-based and GaAs-based QCLs

<table>
<thead>
<tr>
<th>QCL active region</th>
<th>$\lambda$ ($\mu$m)</th>
<th>$T_H$(K)</th>
<th>$k_\perp$ (W/(K $\times$ m))</th>
<th>TBR ($10^{-9}$K/W$\times$m$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InGaAs/AlInAs</td>
<td>8</td>
<td>80</td>
<td>0.6</td>
<td>4.4</td>
</tr>
<tr>
<td>InGaAs/InGaAsSb Epilayer down</td>
<td>4.9</td>
<td>60</td>
<td>1.8</td>
<td>0.75</td>
</tr>
<tr>
<td>InGaAs/InGaAsSb Epilayer up</td>
<td>4.9</td>
<td>60</td>
<td>1.8</td>
<td>0.75</td>
</tr>
<tr>
<td>InGaAs/AlInAs InAs, AlAs $\delta$-layers</td>
<td>4.8</td>
<td>60</td>
<td>2</td>
<td>0.5 – 1.1</td>
</tr>
<tr>
<td>GaAs/Al$<em>{0.33}$Ga$</em>{0.67}$As</td>
<td>9.4</td>
<td>90</td>
<td>5.5</td>
<td>0.48</td>
</tr>
</tbody>
</table>

- Developing new design strategies of QCLs including *smoothed* interfaces and/or *phonon matched* materials will pay off
  - TBR reduction
  - improved thermal management
Electronic properties / wall plug efficiency
[strained In$_{0.61}$Ga$_{0.39}$As/In$_{0.45}$Al$_{0.55}$As QCLs + InAs, AlAs δ-layers]

\[ \alpha = 34.3 \text{ Kcm}^2/\text{kA} \]

\[ R_L = T_L/P = 11.5 \text{ K/W} \]
\[ R_E = T_E/P = 22.0 \text{ K/W} \]
\[ \eta_w = 1 - \Delta T/(P_{\text{in}} \times R_L) \]
\[ \eta_{w_{\text{max}}} = (8.4 \pm 0.7) \% \]
Electron-lattice coupling

<table>
<thead>
<tr>
<th>Heterostructure</th>
<th>λ (µm)</th>
<th>ΔE_C (eV)</th>
<th>α (Kcm²/kA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs/Al₀.₄₅Ga₀.₅₅As</td>
<td>12.6</td>
<td>0.39</td>
<td>44.7</td>
</tr>
<tr>
<td>GaAs/AlAs</td>
<td>11.8</td>
<td>1</td>
<td>29.0</td>
</tr>
<tr>
<td>Ga₀.₄₇In₀.₅₃As/Al₀.₆₂Ga₀.₃₈As₁₋ₓSbₓ epilayer-side</td>
<td>4.9</td>
<td>1.2</td>
<td>10.4</td>
</tr>
<tr>
<td>Ga₀.₄₇In₀.₅₃As/Al₀.₆₂Ga₀.₃₈As₁₋ₓSbₓ substrate side</td>
<td>4.9</td>
<td>1.2</td>
<td>10.8</td>
</tr>
<tr>
<td>InGaAs/AllInAs</td>
<td>4.8</td>
<td>0.62-0.95</td>
<td>34.3</td>
</tr>
<tr>
<td>InAs, AlAs δ-layers</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Comparable active region mean doping in the range 1.5-4.5 cm⁻³
- The electron-lattice coupling increases with the conduction band offset
Planarization w/dielectrics

- Core structure as in Yu, Razeghi et al., APL (2003), $T_H=298$ K, $P=7$ W
- Thermal performance comparable with InP-buried devices
Thermal conductivity of $\text{Si}_3\text{N}_4:Y_2\text{O}_3$

InP (300K)

Si$_3$N$_4$ (300K)

SiO$_2$ (300K)

[K. Watari et al. JMS Lett. (1999)]

CNR-INFM Regional Lab
Planarization of QCLs using Y$_2$O$_3$:Si$_3$N$_4$

[Spagnolo, Lops, Scamarcio, Vitiello, Di Franco, submitted JAP, 2007]

- Improved thermal management
- No lateral current leakage
- Significant reduction in the device thermal resistance
Thermal resistance $R_L = \frac{(T_{\text{max}} - T_H)}{P}$

<table>
<thead>
<tr>
<th>Mounting and processing configuration</th>
<th>Top contact thickness</th>
<th>Insulating material</th>
<th>Planarizing material</th>
<th>$R_L$ (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>“Conventional” Ridge waveguide</td>
<td>0.4 µm</td>
<td>SiO$_2$</td>
<td>----</td>
<td>17.9</td>
</tr>
<tr>
<td>“Conventional” Ridge waveguide</td>
<td>0.4 µm</td>
<td>Si$_3$N$_4$</td>
<td>----</td>
<td>16.3</td>
</tr>
<tr>
<td>InP-Buried</td>
<td>0.4 µm</td>
<td>Si$_3$N$_4$</td>
<td>----</td>
<td>14.1</td>
</tr>
<tr>
<td>Au Electroplated</td>
<td>5 µm</td>
<td>SiO$_2$</td>
<td>----</td>
<td>13.5</td>
</tr>
<tr>
<td>Planarization</td>
<td>0.4µm</td>
<td>SiO$_2$</td>
<td>SiO$_2$</td>
<td>18.4</td>
</tr>
<tr>
<td>Planarization</td>
<td>0.4µm</td>
<td>Si$_3$N$_4$</td>
<td>Si$_3$N$_4$</td>
<td>15.0</td>
</tr>
<tr>
<td>Planarization</td>
<td>0.4µm</td>
<td>Si$_3$N$_4$</td>
<td>Y$_2$O$_3$: Si$_3$N$_4$</td>
<td>13.1</td>
</tr>
<tr>
<td>Planarization + Au Electroplated</td>
<td>5 µm</td>
<td>Si$_3$N$_4$</td>
<td>Y$_2$O$_3$: Si$_3$N$_4$</td>
<td>11.8</td>
</tr>
</tbody>
</table>

- Planarization with suitable dielectrics:
  - Thermal performance comparable with conventional buried or electroplated structures
  - 13% reduction of $R_L$ with respect to reference device [Yu, Razeghi et al. APL 83]
Summary

- Comparison of the electronic and thermal properties of mid-IR QCLs via \( \mu \)-probe PL

- Strategies for the improvement of the thermal performance of mid-IR QCLs operating in the 3-5 \( \mu \m \) range:
  - Reduction of the thermal boundary resistance
    - InGaAs/AlGaAsSb
    - InGaAs/AlInAs + (AlAs, InAs) \( \delta \)-layers
  - Planarization using high-k dielectrics

- \textit{running}:
  - Simultaneous thermal and electrical modeling
  - Design of QCLs w/improved thermal performance